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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,602	04/16/2004	Yee-Chia Yeo	TSM03-0847	1196
25962 7590 05/02/2007 SLATER & MATSIL, L.L.P. 17950 PRESTON RD, SUITE 1000 DALLAS, TX 75252-5793			EXAMINER RAYMOND, BRITTANY L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/826,602	Applicant(s) YEO ET AL.	
	Examiner Brittany Raymond	Art Unit 1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) 1-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 23-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 7/29/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>4/16/2004</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, Claims 23-60 in the reply filed on 4/10/2007 is acknowledged.
2. Claims 1-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 4/10/2007.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 23-60 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 11, 20, 21, and 27 of copending Application No. 10/748076. Although the conflicting claims are not

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identical, they are not patentably distinct from each other because both applications teach an immersion lithography process that uses a protective film (10/748076), which is the same as a barrier layer.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 52 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "gate electrode have" should be changed to "gate electrode has."

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 23-25, 30, and 33-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirayama (U.S. Patent Publication 2006/0141400).

Hirayama ('400) discloses an immersion exposure process comprising: applying

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a resist composition onto a substrate (Paragraph 0137), immersing the substrate in a refractive index liquid and exposing the substrate with light through a mask pattern and the liquid to reach the resist layer (Paragraphs 0141 and 0142), as recited in claims 23 and 30 of the present invention. Example 1 discloses that a resist film having a thickness of 150 nm can be formed on the substrate (Paragraph 0157), as recited in claim 23 of the present invention. Hirayama also discloses that the refractive index liquid can include water (Paragraph 0145), as recited in claim 24 of the present invention. Hirayama states that the light used in the exposure can be an ArF excimer laser, a KrF excimer laser, an F₂ excimer laser, etc. (Paragraph 0144), which is known by one of ordinary skill in this art to have a wavelength of less than 450 nm, as recited in claim 25 of the present invention. Hirayama discloses that the exposed resist film can be developed using an alkaline developer solution (Paragraph 0148), as recited in claim 33 of the present invention. Example 1 discloses that the developer can be tetramethylammonium hydroxide (Paragraph 0160), as recited in claim 34 of the present invention. Hirayama also discloses that a protective film can be formed over the resist film (Paragraph 0140), as recited in claim 35 of the present invention. Hirayama states that the protective film should have no compatibility with the immersion liquid used (Paragraph 0021), and since water is often used as the immersion liquid, this would make the protective film hydrophobic, as recited in claim 36 of the present invention.

Hirayama teaches every limitation of claims 23-25, 30, and 33-36 and thus anticipates the claims.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400) in view of Hirayama (U.S. Patent Publication 2006/0154171).

The teachings of Hirayama ('400) have been discussed in paragraph 8 above.

Hirayama ('400) fails to disclose that a chemically amplified photoresist is used in the immersion lithography process.

Hirayama ('171) discloses a method of forming a resist pattern comprising application of a resist on a substrate, prebaking, exposure, post exposure baking, and developing (Paragraph 0057). Hirayama ('171) also discloses that an immersion lithography step can be added to the process (Paragraph 0060). Hirayama ('171) states that the photoresist used in the process can be made up of a resin that is used for

chemically amplified resists (Paragraph 0067), as recited in claim 28 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used a chemically amplified resist, as suggested by Hirayama ('171), in the process of Hirayama ('400) because Hirayama ('171) teaches that chemically amplified photoresists can work well in immersion lithography processes.

11. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400) in view of Lin (U.S. Patent Publication 2007/0091288).

The teachings of Hirayama ('400) have been discussed in paragraph 8 above.

Hirayama fails to disclose that the optical surface can be silicon oxide or calcium fluoride.

Lin discloses a liquid immersion lithography system used to illuminate light through an immersion fluid that has an objective lens, which can be made up of silicon dioxide, which is an oxide of silicon, or calcium fluoride (Paragraph 0022), as recited in claims 26 and 27 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used silicon oxide or calcium fluoride for the optical surface, as suggested by Lin, in the process of Hirayama ('400) because Lin teaches that this type of material does not react with the immersion liquid used and works well with the type of exposure light used in the present invention.

12. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400) in view of Levinson (U.S. Patent Publication 2005/0037269).

The teachings of Hirayama ('400) have been discussed in paragraph 8 above.

Hirayama ('400) fails to disclose that there is a stage underlying the semiconductor structure and that the stage is immersed in the immersion fluid.

Levinson discloses an immersion lithography apparatus comprising a stage upon which the wafer to be patterned is mounted (Paragraph 0018), as recited in claim 31 of the present invention. Levinson also discloses in Figure 1 that the wafer region is immersed in the immersion fluid. It would be obvious to immerse the stage underlying the wafer in the immersion fluid since the stage is part of the wafer region, as recited in claim 32 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have included a stage underneath the semiconductor wafer and immersed the stage in the immersion fluid, as suggested by Levinson, in the process of Hirayama ('400) because Levinson teaches that a stage is needed to hold the semiconductor substrate and move it around in order to pattern the substrate, and immersing the whole stage allows for the pattern to be formed properly

13. Claims 29, 37-39, 43, 46-50, 53, 55, 57, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent Publication 2005/0123863) in view of Hirayama (U.S. Patent Publication 2006/0141400).

Chang discloses an immersion lithography process comprising: providing a

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material layer, forming a photoresist layer on the material layer, forming a protective layer on the photoresist layer, performing an immersion exposure step to pattern the photoresist layer, developing the photoresist layer, and performing an etching or an ion implantation process to process the material layer by using the photoresist layer as a mask (Paragraphs 0020-0023 and 0027-0028), as recited in claims 37, 46, 49, and 57 of the present invention. Chang states that the material layer can be a dielectric layer or an electrically conductive layer (Paragraph 0020), as recited in claims 50 and 53 of the present invention. Chang also states in the description of related art that in typical immersion lithography processes, the photoresist layer directly contacts with the immersion liquid during the exposure step (Paragraph 0006), as recited in claim 29 of the present invention.

Chang fails to disclose that the photoresist layer can have a thickness of less than about 5000 angstroms, that the immersion fluid is water, that the optical energy comprises light having a wavelength of less than 450 nm, that the semiconductor wafer is immersed in the immersion fluid, that the developing solution can be tetramethylammonia hydroxide, and that the upper portion of the photoresist layer is thermally treated.

The teachings of Hirayama ('400) have been discussed in paragraph 8 above. Hirayama ('400) teaches the recitations of dependent claims 38, 39, 43, 46-48, and 55 of the present invention. Hirayama ('400) also discloses that the protective film is applied to the surface of the resist film (Paragraph 0140), as recited in claim 57 of the present invention. Hirayama ('400) states in Example 1 that the protective film was

formed by mixing a certain composition of materials together, spin coating this onto the resist film, and heating the substrate until the protective film has a certain thickness (Paragraph 0158), as recited in claim 60 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used a photoresist with a thickness less than 5000 Angstroms, water as the immersion fluid, optical energy with a wavelength less than 450 nm, and tetramethylammonia hydroxide as the developing solution, as suggested by Hirayama ('400), in the process of Chang because Hirayama ('400) teaches that this allows for a more accurate liquid immersion lithography process to occur and a more accurately patterned substrate. It also would have been obvious to have immersed the semiconductor wafer in the immersion fluid, as suggested by Hirayama ('400), because Hirayama ('400) teaches that this allows for the exposure light to more accurately travel to the wafer and produce the correct pattern on the wafer. Finally, it would have been obvious to have thermally treated the upper portion of the photoresist, as suggested by Hirayama ('400), because Hirayama ('400) teaches that this is a common technique for forming protective layers on top of photoresist layers.

14. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent Publication 2005/0123863) in view of Hirayama (U.S. Patent Publication 2006/0141400) as applied to claims 29, 37-39, 43, 46-50, 53, 55, 57, 58, and 60 above, and further in view of Lin (U.S. Patent Publication 2007/0091288).

The teachings of Chang and Hirayama ('400) have been discussed in paragraphs 8 and 13 above.

Chang and Hirayama ('400) fail to disclose that the optical surface can be silicon oxide or calcium fluoride.

Lin discloses a liquid immersion lithography system used to illuminate light through an immersion fluid that has an objective lens, which can be made up of silicon dioxide, which is an oxide of silicon, or calcium fluoride (Paragraph 0022), as recited in claims 40 and 41 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used silicon oxide or calcium fluoride for the optical surface, as suggested by Lin, in the processes of Chang and Hirayama ('400) because Lin teaches that this type of material does not react with the immersion liquid used and works well with the type of exposure light used in the present invention.

15. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent Publication 2005/0123863) in view of Hirayama (U.S. Patent Publication 2006/0141400) as applied to claims 29, 37-39, 43, 46-50, 53, 55, 57, 58, and 60 above, and further in view of Hirayama (U.S. Patent Publication 2006/0154171).

The teachings of Chang and Hirayama ('400) have been discussed in paragraphs 8 and 13 above.

Chang and Hirayama ('400) fail to disclose that a chemically amplified photoresist is used in the immersion lithography process.

Hirayama ('171) discloses a method of forming a resist pattern comprising application of a resist on a substrate, prebaking, exposure, post exposure baking, and developing (Paragraph 0057). Hirayama ('171) also discloses that an immersion

lithography step can be added to the process (Paragraph 0060). Hirayama ('171) states that the photoresist used in the process can be made up of a resin that is used for chemically amplified resists (Paragraph 0067), as recited in claim 42 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used a chemically amplified resist, as suggested by Hirayama ('171), in the processes of Chang and Hirayama ('400) because Hirayama ('171) teaches that chemically amplified photoresists can work well in immersion lithography processes.

16. Claims 44 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent Publication 2005/0123863) in view of Hirayama (U.S. Patent Publication 2006/0141400) as applied to claims 29, 37-39, 43, 46-50, 53, 55, 57, 58, and 60 above, and further in view of Levinson (U.S. Patent Publication 2005/0037269).

The teachings of Chang and Hirayama ('400) have been discussed in paragraphs 8 and 13 above.

Chang and Hirayama ('400) fail to disclose that there is a stage underlying the semiconductor structure and that the stage is immersed in the immersion fluid.

Levinson discloses an immersion lithography apparatus comprising a stage upon which the wafer to be patterned is mounted (Paragraph 0018), as recited in claim 44 of the present invention. Levinson also discloses in Figure 1 that the wafer region is immersed in the immersion fluid. It would be obvious to immerse the stage underlying the wafer in the immersion fluid since the stage is part of the wafer region, as recited in

claim 45 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have included a stage underneath the semiconductor wafer and immersed the stage in the immersion fluid, as suggested by Levinson, in the processes of Chang and Hirayama ('400) because Levinson teaches that a stage is needed to hold the semiconductor substrate and to move it around, in order to pattern the substrate, and immersing the whole stage allows for the pattern to be formed properly.

17. Claims 51, 52, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent Publication 2005/0123863) in view of Hirayama (U.S. Patent Publication 2006/0141400) as applied to claims 29, 37-39, 43, 46-50, 53, 55, 57, 58, and 60 above, and further in view of Cheng (U.S. Patent 7176522).

The teachings of Chang and Hirayama ('400) have been discussed in paragraphs 8 and 13 above.

Chang and Hirayama ('400) fail to disclose that the conductive layer can be etched into gate electrodes with the gate electrodes having a minimum dimension of 50 nm or less, and that trenches can be formed in the dielectric layer, with the trenches being filled with a conductor.

Cheng discloses a process for forming a semiconductor device comprising forming gate electrodes with a height of 10 to 200 nm (Column 3, Lines 24-33), as recited in claims 51 and 52 of the present invention. Cheng also discloses that source/drain regions may be formed in the substrate by etching recesses in the

substrate and filling them with materials such as silicon and silicon germanium (Column 4, Lines 1-10), as recited in claim 54 of the present invention. Cheng states that processing techniques such as immersion lithography can be used to process these semiconductor devices (Column 11, Lines 63-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have etched gate electrodes with a minimum dimension of 50 nm or less into the conductive layer, as suggested by Cheng, in the processes of Chang and Hirayama ('400) because Cheng teaches that gate electrodes are often formed on semiconductor substrates and can be formed by immersion lithography. It also would have been obvious to have formed trenches in the dielectric layer and filled these with a conductor, as suggested by Cheng, because Cheng teaches that this is a common process for forming intricate semiconductor devices and can be formed by immersion lithography.

18. Claims 56, 58 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent Publication 2005/0123863) in view of Hirayama (U.S. Patent Publication 2006/0141400) as applied to claims 29, 37-39, 43, 46-50, 53, 55, 57, 58, and 60 above, and further in view of Lee (U.S. Patent Publication 2005/0266683).

The teachings of Chang and Hirayama ('400) have been discussed in paragraphs 8 and 13 above.

Chang and Hirayama ('400) fail to disclose that a plasma treatment, a chemical treatment, or an ion implantation process can be used to treat the upper portion of the photoresist layer.

Lee discloses a photoresist that is used in lithography that can be modified by the following processes: chemical amplification, cross linking, chemical etching, deep ultraviolet treatment, ion implantation, plasma treatment, laser ablation, etc. (Paragraph 0034), as recited in claims 56, 58, and 59 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used chemical amplification, ion implantation, plasma treatment, etc., as suggested by Lee, to form a barrier layer on a photoresist for the immersion lithography processes of Chang and Hirayama ('400) because Lee teaches that these processes work well at modifying a photoresist layer for a lithography process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brittany Raymond whose telephone number is 571-272-6545. The examiner can normally be reached on Monday through Friday, 8:00 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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